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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/751,674	Applicant(s) FARABOSCHI ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2000 and 19 February 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) *1,2,4,5,7,10-14,16 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Declaration and Fee as received on 16 April 2001; Request for Filing Request as received on 16 April 2001; Formal Drawings as received on 16 April 2001; and Supplemental IDS as received on 19 February 2003.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The current abstract is merely a repeat of the independent claims. It does not describe the disclosure sufficiently nor assist readers.

6. The disclosure is objected to because of the following informalities:

a. Please update the information regarding related U.S. Patent Applications found on pages 1-2. Please include the applications' serial numbers and status of the case, i.e. abandoned or allowed.

b. Please revise the Summary of Invention. The current Summary of Invention is merely a repeat of the claims. This does not "set out the exact nature, operation, and purpose" nor provide "material assistance in aiding ready understanding of the patent in future searches of the invention" as set forth in MPEP § 608.01(d).

7. Appropriate correction is required.

Drawings

8. This application, filed under former 37 CFR 1.60, lacks formal drawings for Figures 6 and 7. The informal drawings filed in this application are acceptable for examination purposes. Applicant will be required to submit new formal drawings for Figures 6 and 7. The Formal Drawings submitted on 16 April 2001 is missing page 6 containing Figures 6 and 7 of the Application. The Letter to the Draftsman indicates that page 6 containing Figures 6 and 7 should have been submitted with the Formal Drawings filed 16 April 2001.

9. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: page 22, line 14 element 244 and page 24, line 1 element Register 63. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

10. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 3, elements 342,

343, and 344. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

11. Claims 2 and 11 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claims 1 and 10, which claims 2 and 11 are dependent off of, recite the limitation "routing each of said received complete instructions bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles." The limitation of claims 2 and 11 stating "wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in said each complete instruction bundle" does not further limit claims 1 and 10. The limitation found in claims 1 and 10 quoted above inherently means that the at least address bit is associated with each syllable found in the instruction bundle, since it is associated with the entire instruction bundle.

12. Claims 1, 2, 4, 5, 7, 10, 11, 12, 13, 14, 16, and 19 are objected to because of the following informalities. The corrections are highlighted in italics.

a. Referring to claim 1, lines 5 and 15 and claim 10, lines 11 and 24, please correct the phrases from "where *each said* instruction execution pipelines" and "routing

each said received complete instruction bundles" to read --where *each of said* instruction execution pipelines-- and --routing *each said* received complete instruction bundles--.

b. Referring to claim 2, lines 2 and 5 and claim 11, lines 2 and 5, please correct the phrases from "circuitry *routs each said* received complete" and "in *said each* complete instruction bundles" to read --circuitry *routes each of said* received complete-- and --in *each of said* complete instruction bundles--.

c. Referring to claim 4, lines 2 and 4 and claim 13, lines 2 and 4, please correct the phrases from "circuitry *routs each said* received complete" and "in *said each* complete instruction bundles" to read --circuitry *routes each of said* received complete-- and --in *each of said* complete instruction bundles--.

d. Referring to claim 5, line 3 and claim 14, line 3, please correct the phrase from "routing *said each* received complete instruction bundle" to read --routing *each of said* received complete instruction bundles--.

e. Referring to claims 7 and 16, lines 4-5, 7, and 8, please correct the phrases from "one address bit associated with *said each* complete instruction bundle"; "syllable in *said each* complete instruction bundle"; and "cluster bit associated with *said each* complete" to read --one address bit associated with *each of said* complete instruction bundles--; --syllable in *each of said* complete instruction bundle--; and --cluster bit associated with *each of said* complete--.

f. Referring to claim 12, lines 2 and 4, please correct the phrases from "circuitry *routs each said* received complete" and "in *said each* complete instruction

bundles" to read --circuitry *routes each of said* received complete-- and --in *each of said* complete instruction bundles--.

g. Referring to claim 19, lines 5, 12, 14, 20, and 21, please correct the phrases from "wherein *each the* instruction execution pipelines"; "issuing *complete ones of the instruction* bundles"; "routing *each the* received complete instruction bundles"; "one syllable in *the each* complete instructions bundle"; and "a cluster bit associated with *the each* complete" to read --wherein *each of the* instruction execution pipelines--; --issuing *complete instruction* bundles"; "routing *each of the* received complete instruction bundles"; "one syllable in *each of the* complete instructions bundle"; and "a cluster bit associated with *each of the* complete"

13. Appropriate correction is required.

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 1, 5, 10, 14, and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear what the letters "C", "N", "S", and "L" represent, i.e. whole numbers, real numbers, integers, fractions, etc.

16. Claim 19 recites the limitation "the at least one address bit" in line 17. There is insufficient antecedent basis for this limitation in the claim. At least one address bit has not been established in the claim prior to this occurrence.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 1-3, 8-12, are 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi, U.S. Patent Number 6,167,503 (herein referred to as Jouppi) in view of Vassiliadis et al., U.S. Patent Number 5,051,940 (herein referred to as Vassiliadis).

19. Referring to claims 1 and 10, Jouppi has taught a processing system comprising:

a. A data processor (Applicant's claim 10) (Jouppi column 2, lines 61-64 and Figure 1);

b. A memory coupled to said data process (Applicant's claim 10) (Jouppi column 3, liens 16-25 and Figure 1);

c. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Applicant's claim 10) (Jouppi column 3, lines 16-65 and Figure 1);

d. Wherein said data processor comprises:

i. C execution clusters (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), each of said C execution clusters capable of executing instruction bundles comprising from one to S syllables (Applicant's claims 1 and 10) (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B);

ii. An instruction cache capable of storing a plurality of cache lines, each of said cache lines comprising C*L syllables (Applicant's claims 1 and 10) (Jouppi column 3, lines 58-65; column 4, lines 9-19; Figure 2A; and Figure 2B);

iii. An instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said C execution clusters (Applicant's claims 1 and 10) (Jouppi column 4, lines 25-38; Figure 2A; and Figure 2B); and

iv. Alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said C execution clusters as a function of at least one address bit associated with each of said complete instruction bundles (Applicant's claims 1 and 10) (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

20. Jouppi has not taught

a. An instruction execution pipeline having N processing stages (Applicant's claims 1 and 10);

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10).

21. Vassiliadis has taught

a. An instruction execution pipeline having N processing stages (Applicant's claims 1 and 10) (Vassiliadis column 1, lines 7-40);

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10) (Vassiliadis column 1, lines 7-40); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10) (Vassiliadis column 1, lines 7-40).

22. A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

23. Referring to claims 2 and 11, Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in said each complete instruction bundle (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

24. Referring to claims 3 and 12, Jouppi has taught wherein said alignment and dispersal circuitry routes each received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each complete instruction bundle (Jouppi column 4, lines 53-63; Figure 2A; and Figure 2B).

25. Referring to claims 8 and 17, Jouppi has not taught wherein L=4. Vassiliadis has taught a pipeline with N-stages, which includes 4 stages. In regards to Vassiliadis, it does not matter how many stages the pipeline is. That is the length of a pipeline, i.e. the number of stages, is dependent on how much potential improvement a designer desires (Vassiliadis column 1, lines 12-40). A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

26. Referring to claims 9 and 18, Jouppi has taught wherein C=3 (Jouppi column 5, lines 41-42 and column 10, lines 32-42).

27. Referring to claim 19, Jouppi has taught for use in a data processor C execution clusters (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), each of said C execution clusters capable of executing instruction bundles comprising from one to S syllables (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B), a method of routing instruction bundles into the L lanes in the C execution clusters comprising the steps of:

a. Fetching cache lines from an instruction cache, each of said cache lines comprising C*L syllables (Jouppi column 3, lines 58-65; column 4, lines 9-19; Figure 2A; and Figure 2B);

b. Issuing complete ones of the instruction bundles toward the C execution clusters (Jouppi column 4, lines 25-38; Figure 2A; and Figure 2B); and

c. Routing each of the received complete instruction bundles to a correct one of the C execution clusters as a function of at least one of (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B):

i. At least one address bit associated with each of said complete instruction bundle (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B);

ii. At least one address bit associated with at least one syllable in each of said complete instruction bundle (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B); and

iii. A cluster bit associated with each of said complete instruction bundle (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

28. Jouppi has not taught

a. An instruction execution pipeline having N processing stages (Applicant's claims 1 and 10);

b. Wherein each of said instruction execution pipelines is L lanes wide (Applicant's claims 1 and 10); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Applicant's claims 1 and 10).

29. Vassiliadis has taught

a. An instruction execution pipeline having N processing stages (Vassiliadis column 1, lines 7-40);

b. Wherein each of said instruction execution pipelines is L lanes wide (Vassiliadis column 1, lines 7-40); and

c. Each of said L lanes capable of receiving one of said one to S syllables of said instruction bundles (Vassiliadis column 1, lines 7-40).

30. A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

31. Referring to claim 20, Jouppi has taught wherein C=3 (Jouppi column 5, lines 41-42 and column 10, lines 32-42). Jouppi has not taught wherein L=4. Vassiliadis has taught a pipeline with N-stages. In regards to Vassiliadis, it does not matter how many stages the pipeline is. That is the length of a pipeline, i.e. the number of stages, is dependent on how much potential improvement a designer desires (Vassiliadis column 1, lines 12-40). A person of ordinary skill in the art at the time the invention was made, and as taught by Vassiliadis, would have recognized that pipelining is a standard technique used to improve computer performance (Vassiliadis column 1, lines 13-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the pipelines of Vassiliadis in the device of Jouppi to improve computer performance.

32. Claims 4-7 and 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jouppi in view of Vassiliadis as applied to claims 1 and 10 above, and further in view of Sachs et al., U.S. Patent Number 5,560,028 (herein referred to as Sachs). Jouppi has taught wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

a. Said at least one address bit associated with each of said complete instruction bundle (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B);

b. At least one address bit associated with at least one syllable in each of said complete instruction bundle (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B); and

c. A cluster bit associated with each of said complete instruction bundle (Applicant's claims 7 and 16) (Jouppi column 2, lines 9-13; column 4, lines 25-38 and 53-63; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B).

33. Jouppi has not taught

a. Wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in said each complete instruction bundle (Applicant's claims 4 and 13);

b. Wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundle to any one of said C execution clusters (Applicant's claims 5 and 14); and

c. Wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Applicant's claims 6 and 15).

34. However, Jouppi has taught instruction dispersal circuitry (Jouppi column 2, lines 9-13; column 4, lines 25-38; column 7, lines 6-30; column 8, lines 11-36; Figure 2A; and Figure 2B). Sachs has taught instruction dispersal circuitry

a. Wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least one syllable in said each complete instruction bundle (Applicant's claim 4) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10);

b. Wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundle to any one of said C execution clusters (Applicant's claim 5) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10); and

c. Wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Applicant's claim 6) (Sachs column 3, lines 11-18; column 9, lines 3-6 and 30-62; Figure 8; and Figure 10).

35. A person of ordinary skill in the art at the time the invention was made would have recognized that the instruction dispersal circuitry ensures the correct execution cluster executes

the instruction bundles, thereby ensuring valid and correct data. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the dispersal circuitry of Sachs in the device of Jouppi to ensure valid and correct data.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Vassiliadis et al., U.S. Patent Number 5,502,826, has taught compound instructions with appropriate execution unit flags.

b. Vassiliadis et al., U.S. Patent Number 5,50,932, has taught compound instructions with appropriate execution unit flags.

c. Vassiliadis et al., U.S. Patent Number 5,732,234, has taught compound instructions with appropriate execution unit flags.

d. Miller et al., U.S. Patent Number 5,819,058, has taught compressing and decompressing instructions with bits designating the appropriate execution unit.

e. Blaner et al., U.S. Patent Number 6,029,540, has taught compound instructions with appropriate execution unit flags.

f. D'Arcy et al., U.S. Patent Number 6,079,010, has taught compound instructions with appropriate execution unit flags.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

39. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li

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